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Third Semester B.E. Degree Examination, June/July 2017
Logic Design

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1 a. What are universal gates? Realize basic gates using only NAND gates. (06 Marks)
- b. An unsymmetrical waveform is high for 2 msec and low for 5 msec. Find the frequency and duty cycle of the waveform. (04 Marks)
- c. State DeMorgan's theorem for two variables and prove the same using perfect induction. (06 Marks)
- d. Using structural modeling write the verilog code for the circuit shown in Fig.Q1(d). (04 Marks)

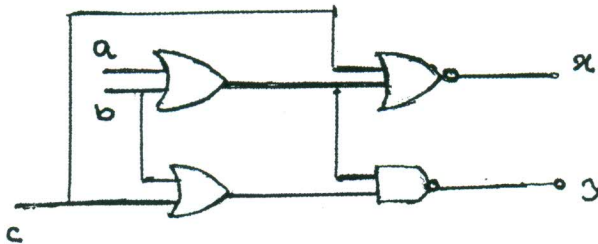


Fig.Q1(d)

- 2 a. Reduce the following function using Karnaugh Map technique.
 - i) $f(a, b, c, d) = \sum m(5, 6, 7, 2) + d(4, 9, 14, 15)$
 - ii) $f(w, x, y, z) = \pi M(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$. (10 Marks)
- b. Find all the prime implicants of the function using Quine Mcklusky method for :
 $f(a, b, c, d) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ (10 Marks)
- 3 a. Implement the given Boolean function using 8 : 1 MUX :
 $f(p, q, r, s) = \sum m(0, 1, 3, 5, 7, 11, 12, 13, 14)$. (08 Marks)
- b. Using 3 : 8 decoder and external OR gates realize the following Boolean expression :
 $F_1(A, B, C) = \sum m(1, 2, 3, 5)$; $F_2(A, B, C) = \sum m(4, 6, 7)$. (06 Marks)
- c. Implement the given Boolean function using PLA :
 $X = A'B'C + AB'C' + B'C$
 $Y = A'B'C + AB'C'$
 $Z = B'C$. (06 Marks)
- 4 a. Explain the characteristics of ideal clock. (04 Marks)
- b. With transfer characteristics, explain how Schmitt trigger converts a random waveform into a rectangular waveform. (06 Marks)
- c. Explain the working of SR flipflop using NOR gates. What are the draw backs of SR flipflop? How JK flipflop is obtained from SR flipflop? (10 Marks)



PART - B

- 5 a. Using negative edge triggered JK flipflops, draw the logic diagram of a 4-bit serial-in-serial-out shift register. Draw the waveform to shift the binary number 1010 into this register. Also draw the waveform for four clock transitions when $J = K = 0$ (assume register has stored 1010 in it). (10 Marks)
- b. Explain 4-bit programmable sequence detector using EX-OR gates with a neat diagram. (05 Marks)
- c. Write verilog code for Johnson counter. (05 Marks)
- 6 a. What do you mean by lockout condition in counters? Using JK flipflops design a self correcting mod-6 counter. (12 Marks)
- b. Design synchronous mod-8 up counter using JK flipflop. (08 Marks)
- 7 a. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig.Q7(a). (08 Marks)

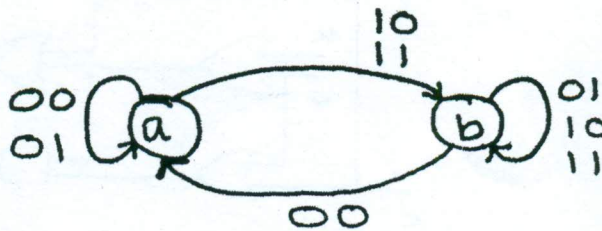


Fig.Q7(a)

- b. Reduce the following state table using implication table method with a neat figure.

Present state		Next state			Present output	
		x = 0	x = 1		x = 0	x = 1
a	-----	a	b	-----	0	0
b	-----	c	d	-----	0	0
c	-----	e	f	-----	0	0
d	-----	b	a	-----	0	1
e	-----	c	d	-----	0	0
f	-----	d	a	-----	0	1

(12 Marks)

- 8 a. Discuss the working of successive approximation analog to digital converter. (06 Marks)
- b. What is a binary ladder? Explain the same with a digital input of 1000. (06 Marks)
- c. Explain continuous AD conversion technique with an example. (08 Marks)
